

CLAIMS:

1. A method for processing an information based on a sequence of instructions, said method comprising the steps of:
 - a) detecting a repeated sub-sequence in said sequence of instructions;
 - b) providing an index information indicating the repetition frequency of said repeated sub-sequence; and
 - c) determining an allocation between a processing resource and said repeated sub-sequence based on said index information.
2. A method according to claim 1, further comprising the step of generating an instruction containing said index information, and adding said instruction to said sequence of instructions.
3. A method according to claim 1 or 2, wherein said index information comprises an integer number set in proportion with a ranking of said repetition rate of said repeated sub-sequence compared to the repetition rate of other detected repeated sub-sequences.
4. A method according to claim 3, wherein said allocation is determined by comparing said integer number with the number of available processing resources.
5. A method according to claim 4, wherein all repeated sub-sequences for which said integer number is smaller than said number of available processing resources are allocated to a selected processing resource.
6. A method according to any one of the preceding claims, wherein said index information comprises an information indicating the number of instructions in said repeated sub-sequence.
7. A method according to any of the preceding claims, further comprising the step of generating an instruction for deleting said repeated sub-sequence, if said repeated sub-

sequence is no longer detected for a predetermined time period, and resetting a processing unit to which said deleted repeated sub-sequence was allocated.

8. A method according to any one of the preceding claims, further comprising the
5 step of generating an instruction for specifying processing registers used by said repeated sub-sequence, and using said instruction for locking said specified processing registers.

9. A method according to claim 2, further comprising the step of activating a
10 processing resource when said instruction containing said index information indicates that the corresponding repeated sub-sequence has already been allocated to said processing resource.

10. A method according to claim 9, wherein said activating step comprises the
step of programming said processing resource according to said corresponding repeated sub-
sequence, or uploading said corresponding repeated sub-sequence to a memory of said
15 processing resource.

11. A method according to any one of the preceding claims, further comprising the
step of signalling the presence of external processing units to a central processing unit, and
counting the number of available external processing units based on said signalling.
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12. An apparatus for processing an information based on a sequence of
instructions, said apparatus comprising:

a) detecting means for detecting a repeated sub-sequence in said sequence of
instructions, and for providing an index information indicating the repetition frequency of
25 said repeated sub-sequence; and

b) resource control means for allocating said repeated sub-sequence to a
processing resource based on said index information.

13. An apparatus according to claim 12, further comprising connecting means for
30 connecting at least one external processing unit to which said repeated sub-sequence can be
allocated.

14. An apparatus according to claim 13, further comprising a memory table for storing an allocation information indicating an allocation between said at least one external processing unit and corresponding repeated sub-sequences.

5 15. An apparatus according to claim 13 or 14, wherein said apparatus is a digital signal processor and said at least one external processing units are processor cores and/or configurable logic blocks.

10 16. An apparatus according to any one of claims 13 to 15, further comprising means for determining the number of said at least one external processing units connected to said connecting means.

15 17. An apparatus according to any one of claims 13 to 16, further comprising mapping means for mapping said repeated sub-sequence to an available one of said at least one external processing unit based on said index information.

20 18. A compiler for providing an output sequence of instructions to be used for processing an information, said compiler being arranged to detect a repeated sub-sequence in said output sequence of instructions and to provide an index information indicating the repetition frequency of said repeated sub-sequence.

19. A compiler according to claim 18, wherein said compiler is arranged to add to said repeated sub-sequence an instruction specifying said index information.

25 20. A compiler according to claim 19, wherein said additional instruction is added so as to precede said repeated sub-sequence.

30 21. A compiler according to any one of claims 18 to 20, wherein said compiler is arranged to add to said output sequence an instruction for indicating that said repeated sub-sequence is not used anymore.

22. A compiler according to any one of claims 18 to 21, wherein said compiler is arranged to add to said output sequence an instruction for allocating at least one processing register means until said repeated sub-sequence is finished.

23. A compiler according to any one of claims 18 to 21, wherein said compiler is arranged to determine a ranking of repeated sub-sequences based on their repetition rate.